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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,791	12/05/2001	Toshimitsu Tamagawa	103213-00042	2283

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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER

VILLECCO, JOHN M

ART UNIT	PAPER NUMBER
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2622

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/001,791

Applicant(s)

TAMAGAWA, TOSHIMITSU

Examiner

John M. Villecco

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11, 12 and 14 is/are allowed.
- 6) ☒ Claim(s) 9 and 13 is/are rejected.
- 7) ☒ Claim(s) 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant has amended claim 11 to overcome the claim objection presented in the previous office action.
2. Additionally, applicant has amended each of independent claims 9, 11, 13, and 14 to recite some variation the limitation of a signal output line switching circuit connected between the plurality of first (and second) signal output lines and the output circuit and has presented arguments stating that Tseng fails to disclose the claims, as amended. In particular, the applicant argues on page 16 of the response that Tseng fails to specifically disclose a signal output switching circuit connected between the plurality of signal output lines and the output circuit. This amendment appears to overcome the 102 rejection based on Tseng in the previous office action. Additionally, applicant argues on page 17 that Tseng fails to disclose how to reduce the parasitic capacitance within an IC chip or how to reduce an overall parasitic capacitance of the path of the signal output leading from the photoelectric conversion element S to the output circuit. However, this limitation cannot be found anywhere in the claims and, as such, will not be duly considered. However, the examiner has found additional art that can be used in rejecting claim 9 and 13. Please see the new grounds of rejection presented on the following pages.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Miyazawa (U.S. Patent No. 4,661,860).

5. Regarding *claim 9*, Miyazawa discloses an image reader for a facsimile device or the like, capable of reading out the photoelectric charges in groups. More specifically, Miyazawa discloses a plurality of image reading photoelectric conversion elements (photodiodes, PD) divided into a plurality of groups (BL1...BLn), a read selection circuit (switches, SWnm) for sequentially selecting the plurality of image reading photoelectric conversion elements and reading a photoelectric conversion signal from the selected image reading photoelectric conversion element, a plurality of signal output lines (output lines connected to each of the groups) by way of which the photoelectric conversion signal is transmitted, each of the plurality of signal output lines being independently provided from each other and corresponding to each of the plurality of groups, an output circuit (amplifier, AM), and a signal output line switching circuit (switches, SL1...SLn) connected between the plurality of signal output lines and the output circuit (amplifier, AM) for sequentially selecting among the plurality of signal output lines to lead the photoelectric conversion signal to the output circuit. Miyazawa discloses that the selection switches (SL1...SLn) are sequentially activated using clocking signals to output pixels of each block. Inherently the output of the clocking signals would have to be carried out by a logic circuit. See Figures 2 and 3 and column 2, lines 22-60.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (U.S. Patent No. 5,724,094) in view of Miyazawa (U.S. Patent No. 4,661,860).**

8. Regarding *claim 13*, As for claim 13, Tseng discloses a contact image sensor utilizing differential voltage pickoff. More specifically, Tseng discloses a multiple chip IC for reading an image (Figure 10); a plurality of image reading photoelectric conversion elements (pixels S1-Sn and dl-dn), a read selection circuit (shift register, col. 3, lines 54-57) for sequentially selecting the plurality of image reading photoelectric conversion elements and reading a photoelectric conversion signal from the selected image reading photoelectric conversion element; a plurality of signal output lines by way of which the photoelectric conversion element signal is transmitted, each of the plurality of signal output lines corresponding to and independently provided for each of the plurality of groups (as shown in Figure 8 each of the pixels outputs its signal through though an output. Furthermore, Tseng discloses the use of a clock signal. See column 4, lines 22-34. Each chip of Tseng includes a clock input (ϕ clock) to the system that includes a clock input terminal for inputting the clock signal into the device. Furthermore, as previously discussed Tseng discloses the use of an end of scan (EOS) feature, which operates as a start trigger. As shown in Figure 8, the EOS signal is input and output from each of the plurality of

chips. Therefore each chip would include an input and output terminal for receiving the EOS signal.

Tseng, however fails to specifically disclose that the plurality of photoelectric conversion elements are divided into plurality of groups, a plurality of signal output lines for each of the groups, a signal output line switching circuit connected between the signal output lines and the output circuit, or a logic circuit for controlling the signal output line switching circuit.

Miyazawa, on the other hand, discloses that it is well known in the art to provide an image sensing chip with a plurality of photoelectric conversion elements divided into a plurality of different groups. More specifically, Miyazawa discloses a plurality of image reading photoelectric conversion elements (photodiodes, PD) divided into a plurality of groups (BL1...BLn), a read selection circuit (switches, SWnm) for sequentially selecting the plurality of image reading photoelectric conversion elements and reading a photoelectric conversion signal from the selected image reading photoelectric conversion element, a plurality of signal output lines (output lines connected to each of the groups) by way of which the photoelectric conversion signal is transmitted, each of the plurality of signal output lines being independently provided from each other and corresponding to each of the plurality of groups, an output circuit (amplifier, AM), and a signal output line switching circuit (switches, SL1...SLn) connected between the plurality of signal output lines and the output circuit (amplifier, AM) for sequentially selecting among the plurality of signal output lines to lead the photoelectric conversion signal to the output circuit. Miyazawa discloses that the selection switches (SL1...SLn) are sequentially activated using clocking signals to output pixels of each block. Inherently the output of the clocking signals would have to be carried out by a logic circuit. See Figures 2 and 3 and column 2, lines

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22-60. Miyazawa discloses that this arrangement preserves a desirable dynamic range (col. 2, lines 22-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to drive the output of image signal of Tseng in a manner similar to Miyazawa so that a desirable dynamic range is maintained.

The combination of Tseng and Miyazawa, however, fails to specifically disclose the use of an A/D converter for converting the signal from the output circuit into a digital signal.

Official Notice is taken as to the fact that it is well known in the art to convert analog signals into digital signals after readout from an image sensor. It is well known in the art that digital signals have advantages over analog signals in that they are less susceptible to interference, signal loss, and noise. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to convert the analog output of the device in Tseng to a digital signal so that it is less susceptible to noise.

Allowable Subject Matter

9. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 10, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest that the initialization selection circuit initializes

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the selected image reading photoelectric conversion element during a last half of a period of the clock period and during a first half of a next clock period.

11. Claims 11, 12, and 14 are allowed.

12. Regarding claims 11 and 14, the primary reason for allowance is that the prior art fails to teach or reasonably suggest an IC chip including a signal output line switching circuit connected between the plurality of first signal output lines and the output circuit for switching among the plurality of first output lines and connected between the plurality of second signal output lines for sequentially selecting among the plurality of second signal output lines and a logic circuit for controlling the signal output line switching circuit to switch from a first signal output line currently selected to a first signal output line subsequently selected and from a second signal output line currently selected to second signal output line subsequently selected after the each of the previous groups are read out.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

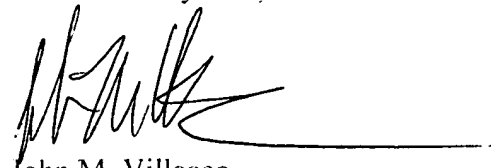
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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (571) 272-7319. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



John M. Villecco
February 6, 2007